REMARKS

Claims 1-5 are pending.

The Examiner takes the position that the argument submitted in the August 27, 2004 amendment did not address the rejection of claims 1-5 because the subject matter of claims 1-5, as they then appeared, was not supported in the Specification. Therefore, claims 1-5 were rejected under §112 (first paragraph) as not being supported in the Specification. In the Final Rejection the Examiner maintained the rejection of claims 1-5 as unpatentable under §103 over the admitted prior art (APA) of pages 2-7 of the Specification in view of Le, et al., U.S. 6,578,169 as set forth in the Office Action of June 2, 2004 has been maintained.

In the final Rejection, the Examiner rejected claim 6 under §112 (first paragraph). Claim 6 is proposed to be cancelled.

Claims 1-5 are now rejected under §112 (second paragraph) as being indefinite for various language problems. This, in some measure, relates to the question of support for the claim subject matter raised in the June 2, 2004 Office Action and the language used.

It is demonstrated below, in responding to the §112 (second paragraph) rejection of claims 1-5, that the subject matter of claims 1-5 was and is supported in the Specification and that these claims are definite in form.

Claims 1-5 also are objected to for various language problems. The claims as proposed to be amended, satisfy these objections.

The Remarks first addresses the §112 (second paragraph) rejections for each of claims 1-5 and then returns to the rejection on the art.

Claim 1. To explain the semiconductor test apparatus of the present invention, it comprises an input data generating unit for generating the measurement data that is to be applied to the semiconductor test device based on first input measurement conditions. There is an expected data generating unit for generating expected data that would be expected from testing the semiconductor device using the measurement data under the first input

measurement conditions. It should be understood that there is different measurement data for different types of semiconductor devices. When the measurement data is applied to conduct a test, measurement result data from the test is produced. There is a determination unit for comparing the measurement result data with the expected data, for determining whether the function of the test semiconductor device (the one under test) is a pass or a failure. There also is a data log system unit for writing in a time sequence into a log memory "associated data", i.e., the data associated with the semiconductor under test. The "associated data" includes the measurement data, expected data, and the determination result data.

The input data generating unit, set externally by an operator, presets the data log system with a write termination condition for terminating writing into the data log memory when the test result of a test semiconductor device is a failure or when all test results of the function test of the test semiconductor device have been completed. The input data generating unit also presets a write extension condition for extending the writing into the data log memory when the test result of a test semiconductor device becomes a failure before all function tests for the test semiconductor device have been completed or when the address of the data log memory has not been completed.

The data log system continues the writing of subsequent associated data of the test semiconductor device into the log memory over an extended period of time according to the preset write extension condition until the write termination condition is satisfied.

To further understand the operation of the apparatus, reference is made to page 13, lines 11-19 of the Specification. This part of the Specification describes that the data log system continues the writing of the associated data (measurement data, measurement expected data and determination result data) to the log memory over the range of the extended time that the input write extension conditions indicate even after the write termination conditions are satisfied. That is, the extended time writing continues even after any of the associated data or the address of the log memory have matched the write termination conditions that have been set in advance by the input generating unit.

Furthermore, as described on page 15, lines 1-16 of the Specification, the data log system unit 16 determines the condition of whether or not the write termination conditions that have been set from the input generating unit are met, and if the determination result data SR has become a Fail, the processing returns to step S47 to continue the writing.

Claim 1 is proposed to be amended to simplify the language by canceling the last clause of claim 1 and inserting:

> wherein said input data generating unit presets said log system with a write termination condition for terminating writing into the data log memory when the test result of a test semiconductor device is a failure or when all test results of the function test of a test semiconductor device have been completed, and said input data generating unit also presets a write extension condition for extending the writing into the data log memory when the test result of a test semiconductor device becomes a failure before all function tests for the test semiconductor device have been completed or when the address of the data log memory has not been completed,
>
> wherein said data log system continues the writing of subsequent associated data of the test semiconductor device into the log memory over an extended period of time according to the write extension condition until said write termination condition is satisfied.

Therefore, claim 1 is now more consistent with the language used in the Specification and is definite in form.

Claim 2. The Examiner rejected claim 2 as being indefinite because of the indefinite expression "the failure". This phrase has been eliminated. In addition, the phrase "wherein the second measurement data includes results of a measurement for analysis of the fail" was deleted.

Claim 3. The Examiner rejects claim 3 as being indefinite because "the test device" in line 4 is indefinite. To overcome this, claim 3 is proposed to be amended by deleting reference to two test devices expressed as having first and second result data as previously set forth in parent claim 1. It should be understood that the test apparatus of the application carries out tests for many semiconductor devices in sequence and the data log

system writes measurement results of a series of test semiconductor devices, as shown in Fig. 2. As shown, the writing is terminated if a test of a semiconductor device is determined as a failure. However, if the associated data of a device which is determined to be failure is not written in the data log memory, the associated data of the device that has failed is written in the data log memory according to the preset writing extension condition in order to be capable of analyzing reasons for the failure afterward.

Claim 4. The Examiner considers the phrase "the associated data" limitation of line 3 as indefinite. The phrase "associated data" is referred to and defined in the fourth clause of amended claim 1.

Claim 4 addresses the situation that while tests for a plurality of semiconductor devices are carried out, the test data is written in the log memory. However, since the data log memory has a predetermined address length, it is not possible to continuously write the test results and respective associated data. If a predetermined address for writing is fully occupied by the test result data and respective associated data, test results and associated data of the subsequent semiconductor devices that are tested is carried out so as to overwrite the memory starting from the log memory head address. Therefore, it is not appropriate to limit the number of semiconductor devices under test to only first and second devices.

The subject matter of claim 4 is directed to the procedure that, while a series of test semiconductor devices are tested and the addresses of the data log memory are fully occupied by the preceding test results, test results and associated data of a subsequent test semiconductor device are overwritten from the head address of the data log memory.

Claim 5. The Examiner rejects claim 5 because of the phrase "the test semiconductor device" limitation as not being clear as to which of two test devices in claim 1 are being referred.

Claim 5 is proposed to be amended to make it clear that the data being written corresponds to the test semiconductor device being tested. The "associated data feature" is discussed above. Amended claim 1 does not specify the semiconductor test devices under test to be the first and the second test devices.

It is submitted that all of the claims are now definite in form and fully supported by the Specification as originally filed.

The substantive rejection of claims 1-5 over the admitted prior art in view of Le is now addressed.

The conventional semiconductor test apparatus as described in the opening portion of the Specification comprises a function test unit 101, an input data generating unit 102 for generating measurement input data (SI) for use with a test semiconductor device, an expected data generating unit 103 for generating measurement expectation data (SP) responding to the measurement input data (SI), and a determination unit 104 that compares the measurement result data (SO) of the test semiconductor device with the measurement expectation data (SP) and determines whether the test semiconductor device is a pass or failure. There also is a data log system unit 106 that writes into the data log memory in a time sequence "associated data" that includes the determination result data (SR), measurement result data (SO), measurement expectation data (SP), and measurement input data (SI) as conceptually shown in Fig. 2.

The operator of the test apparatus operates the input data generating unit to set the write termination conditions in the data log system unit 106 for terminating the writing into the data log system unit when the determination result becomes a failure, or all of the test items for the test semiconductor device the address of the data log memory unit reaches the designated final address. The next data is written into the data log memory from the head address, overwriting data associated with the subsequent testing.

Accordingly, in the conventional system, test data including SI, SP, SO and SR are sequentially recorded in the data log memory along a time axis, and when the memory address reaches the end address, the next data is stored from the head address overwriting the previous data in a cyclic manner. In addition, when the determination result data indicates failure, the writing to the data memory is terminated according to the preset write termination conditions. The conventional test apparatus is constructed in order to carry out functional tests and for obtaining the determination results quickly.

The semiconductor test apparatus of the subject application includes the same elements as the conventional apparatus including the data log memory. In the present invention, the user (operator) also sets into the log memory the write termination conditions for the test device 15, as shown in Fig. 1. In addition, as not shown or suggested in the conventional apparatus, the user presets write extension conditions into the log memory. The test data including SI, SP, SO and SR are written in the memory, in the same time sequential cyclic manner as the conventional apparatus and when all items of the functional tests are completed, the writing is terminated.

The distinct and novel feature of the present invention is that the log memory also has preset into it in advance the write extension condition. The write extension condition corresponds to a period of time to extend the writing in the data log memory. That is, when the test result shows failure, the writing is terminated because it matches to the write termination condition. According to the ability to have the write extension condition, the functional test data, including SI, SP, SO and SR, after determination of the failure is continuously written by incrementing the address for a preset period of extension time. This permits the apparatus to log the functional data of the failed semiconductor device and to carry out functional analysis and evaluation of a failed semiconductor device.

Le discloses a semiconductor test system, comprising a pattern memory for producing a test pattern for the semiconductor device under test (DUT), means for evaluating the output signal of the DUT, a failure data memory for storing failure data, after compacting the data for failure device that occurred, in a plurality of addresses for storing failure data occurred for each group of addresses. Le also discloses a semiconductor test device, including the test pattern generation unit, a function determination unit, and log memory for storing the test result address by address.

However, Le does not disclose the data log system of the present invention, in which, which has both a write termination and a write extension capability.

As should be clear, the combination of references does not meet the novel and advantageous subject matter set forth in claim 1 and its dependent claims 2-5. Therefore, these claims are patentable and should be allowed.

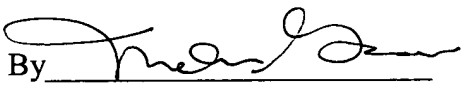
In view of the above, each of the presently pending claims in this application is believed to be in condition for allowance. No new issues are raised. The amendment is directed primarily to clearing up objections to the language of the claims. Accordingly, the Amendment After Rejection should be entered and the Examiner is respectfully requested to pass this application to issue.

If the Amendment After Final Rejection is not entered as placing the application in condition for allowance, then its entry is requested for purposes of appeal.

Prompt and favorable action is requested.

Respectfully submitted,

Dated: April 27, 2005

By 

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